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EXAMINER	
DOAN, DUC T	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,448	FLOMAN ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,33 and 34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22,33-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-34 have been presented for examination in this application. In response to the last office action, claims 1-9,11,14,16-18, 20-22,33-34 were amended, claims 23-32 have been canceled. As the result, claims 1-22,33-34 are pending in this application.

Claims 1-22,33-34 are rejected.

Applicant's remarks filed 3/2/07 have been fully considered but they are not persuasive. Therefore, the rejections from the previous office action are respectfully maintained, with changes as needed to address the amendments.

Claim Objections

Claim 6 is objected to because of the following informalities:

As in claim 6 line 2, the recitation "..least one of of" should be replaceb by "..least one of".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4,8,12,20-22,33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (US 6792499), in view of Lin (US 7032105) and further in view of Eaton et al (2005/0128322).

As in claim 1, Ganton discloses a memory module comprising: a fast nonvolatile random access memory, responsive to a command/data signal provided by a processor (Ganton's Fig 1 discloses a fast non-volatile random access memory, in which data in #115 loading into RAM #120 responsive to processor CPU using a command address data signals, see Ganton's paragraphs 11, 29; Ganton further discloses the memory #115), configured to provide a permanent storage of information before said command/data signal is provided, configured to execute a command comprised in said command/data signal using said permanently stored information (Ganton's paragraph 25 non-volatile memory provides storages for operating systems, program code, applications, radio calibration parameters and phone books information, Ganton's paragraph 30 further discloses executing using code permanently stored in the non-volatile random access memory), for providing a direct communication between said non-volatile random access memory and the processor (Ganton's Fig 1, command address/data signal providing direct communication between non-volatile memory and processor); and

Ganton does not expressly disclose a double interface configured to communicate with said processor. Ganton discloses the memory controller includes well known in the art convert circuitry to converting different protocol for interfaces with different memory devices such as non-volatile, sram, sdram etc.. Ganton further discloses using different clock edges to convert

and clocking data in different memory interfaces. Ganton does not expressly disclose the double rate DDR type interface. However, Lin discloses a memory controller having SDRAM and DDR interface conversion circuitry (Lin's column 4 lines 35-39, Fig 1: #74). It would have been obvious to one of ordinary skill in the art at the time of invention to include conversion circuit and the memory storing method as suggested by Lin in Ganton's system to convert load/store commands issued by the CPU into appropriate memory access commands for accessing DDR dynamic random memory, thereby providing the system with a fast efficient method to store data into DDR DRAM in a permanent manner, see Lin's column 3 lines 57-67; Lin's column 3 lines 57-62 further discloses a mechanism wherein a memory device, for example Lin's Fig 3: #68 SDRAM, readily to be a non-volatile memory by having an uninterruptible power supply (i.e battery)),

Ganton and Lin do not expressly disclose the claim's aspect of electronic device's parts. However, Eaton discloses an electronic device (Eaton's paragraph 1, cellular phone, PDA etc..) capable of combining several parts including memory module part (Eaton's Fig 2: #144 paragraph 15 hierarchical memory in mobile device, ROM EEPROM RAM etc..) processor part (Eaton's Fig 2: #152), speaker part (Eaton's Fig 2: #156). It would have been obvious to one of ordinary skill in the art at the time of invention to include the method of combining parts in an electronic device as suggested by Eaton in Ganton's system modified by Lin which operates parts in a combination manner, thereby further providing new features while maintain the small size and portability of the electronic device (Eaton's paragraph 2).

As in claim 2, Ganton discloses the memory controller having converting circuitry to convert different protocols for interfacing with different memory devices such as non-volatile,

sram, sdram etc.. Ganton further discloses of using different clock edges to convert and clocking data in different memory interfaces. Ganton does not expressly disclose the double rate DDR type interface. However, Lin discloses a memory controller having SDRAM and DDR interface conversion circuitry (Lin's column 4 lines 35-39, Fig 1: #74). It would have been obvious to one of ordinary skill in the art at the time of invention to include conversion circuit and the memory storing method as suggested by Lin in Ganton's system to convert load/store commands issued by the CPU into appropriate memory access commands for accessing DDR dynamic random memory, thereby providing the system with a fast efficient method to store data into DDR DRAM in a permanent manner, see Lin's column 3 lines 57-67).

As in claims 3-4, wherein the fast non-volatile random access memory is configured to provided a temporal storage of data (claim 3, Ganton's paragraph 28 discloses non-volatile random access memory stores temporary data such as recent call lists); wherein said fast non-volatile random access memory comprises an information storage area configured to permanently store said information; and a temporal data storage area for the temporal storage of said data (claim 4, Ganton's paragraph 28 discloses the non-volatile storage stores permanently information such as operating system and temporary data such as phone book, recent call lists, and a temporal data storage area/memory configured to store said data, Ganton's paragraph 28 lines 3-15. Note that SDRAM is readily a non-volatile memory by having a non-interrupt power source, see Lin's Fig 3: #68 SDRAM).

As in claim 8, Ganton discloses wherein said information comprises an application program for operating an electronic device (Ganton's paragraph 25 discloses information

comprises program codes, applications, radio calibration parameters and phonebook information).

Claim 12 rejected based on the same rationale as of claim 2.

Claim 20 rejected based on the same rationale as of claim 1.

As in claims 21-22, Ganton discloses a power and reset block, for resetting said processor and for resetting said fast non-volatile random access memory; wherein said electronic device is a portable electronic device, a mobile electronic device or a mobile phone (claim 21, power supplying and resetting circuitry for a system is represented in Ganton's Fig 7: #26, paragraph 4 the device is a mobile phone etc..).

Claim 33 rejected based on the same rationale as of claim 1

Claims 5,7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (US 6792499), Lin (US 7032105), Eaton et al (2005/0128322) as applied to claim 4 and in view of Witek et al (US 7093153).

As in claim 5, Ganton, Lin, and Eaton do not expressly disclose at least one register for setting operating parameters of the fast non-volatile random access memory or to protect said data or said information during said execution. However, Witek discloses a controller having set of registers configured to set operating parameters of the memory devices such as sdram, sram, and non-volatile memory devices (Witek's column 5 lines 40-65). It would have been obvious to one of ordinary skill in the art at the time of invention to include registers sets in memory controllers as suggested by Witek in Ganton's system modified by Lin and Eaton to allow hardware logic to optimize the memory devices operation dynamically in an efficiently manner,

thereby to further reduce the power consumption of the overall system (Witek's column 2 lines 1-10). Witek's column 5 lines 55-64 further discloses the set of register (i.e address region control registers) are used to protect write to a region, for example write to a read only region will be protected.

As in claim 7, Witek's column 5 lines 55-64 further discloses the set of register (i.e address region control registers) are used to protect write to a region, for example writing to a read only region will not be allowed (i.e write protection).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (US 6792499), Lin (US 7032105), Eaton et al (2005/0128322), Witek et al (US 7093153) as applied to claim 5 and in view of Micron (Micron's synchronous DRAM 256Mb: x4, x8, x16 SDRAM features)

As in claim 6, Witek further discloses wherein said operating parameters comprises at least one of timings for a particular frequency, and frequency ranges with a corresponding core voltage range (Witek's Fig 1 discloses a phase lock loop logic provides timing for a particular frequency, and providing clocks in a range of frequencies. Witek's column 6 lines 8-50 further discloses the operating parameters are used to optimizing the devices' operating frequencies corresponding to the core voltages being used in the devices, thus the overall power consumption of the system can be reduced). None of Ganton, Lin, Eaton and Wiltek expressly discloses the frequency ranges corresponding to a core voltage for a memory. However, Micron's page 1, table 2 discloses any memory device with a core frequency capable of operating in a range of frequencies. For example, Table 2: a memory device having an operating frequency ranges 167

MHz to 100 Mhz corresponding to a core voltage for a memory device. It would have been obvious to one of ordinary skill in the art at the time of invention to provide frequency ranges information corresponding to a core voltage of a memory device as suggested by Micron in Ganton's system thereby further allowing the system to optimize the data throughput accordingly to the frequency ranges of the memory device (see Micron's table 2).

Claims 9-11,13-18,34 rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (US 6792499), Lin (US 7032105) and Eaton et al (2005/0128322) as applied to claim 1, and in view of Pua et al (US 2005/0041473).

As in claim 9, Ganton, Lin and Eaton do not expressly disclose the claim's detail of a mass memory, However, Pua's Fig 2 discloses a memory controller (Pua's Fig 2: #12 controlling IC) comprises a mass memory configured to provide (memory attaching to the Fig 2: #131 NAND IC terminal) more storages to store information in response to a command/information signal from the memory controlling integrate circuitry Fig 2: #12 IC (see Pua's paragraph 20 lines 13-16). It would have been obvious to one of ordinary skill in the art at the time of invention to include memory controller capable of controlling multiples memory devices as suggested by Pua in Ganton's system modified by Lin and Eaton, thereby extra memory capacity can be readily added in the system (Pua's paragraph 20 lines 13-16). Similarly, Ganton further discloses that an application-specific integrate circuit is employed to provide command/information signal to memory device (Ganton's Fig 5, paragraph 33).

As in claim 10, Pua's Fig 2 discloses wherein said further information is provided to say fast non-volatile random access memory (information of memory attaching to Pua's Fig 2: #131 is provided to non-volatile memory Fig 2: #13).

As in claim 11, Pua discloses information in the extend memory attached to Pua's Fig 2: #131, is provided to the non-volatile random access memory (Pua's Fig 2: #13), this information will be used/processed by the processing element (Ganton's Fig 5: #525,paragraph 34). Ganton further discloses that the memory area, Ganton's Fig 1: #120 is configured to execute a further command comprises in said command/data signal using said further information, for example information in Ganton's Fig 1: #115 memory area).

As in claim 13, Ganton discloses a non-volatile random access memory integrate circuit package comprises the application specific integration circuit (Ganton's Fig 1: #105, serial memory interface controller), the mass memory and the fast non-volatile random access memory (Ganton's Fig 1: #115), Pua further disclose a mass memory readily attached to the system to increase the total capacity of the memory system (memory attached to Pua's Fig 2: #131) or the application specific integration circuit (Ganton's Fig 1: #105, serial memory interface controller), and the fast non-volatile random access memory (Ganton's Fig 1: #115), or the mass memory and the non-volatile random access memory (Ganton Fig 3, paragraph 31, discloses another embodiment in which the processor having extra circuitry to provide reading/processing boot code in the onboard ROM Fig 1: #307, thus the circuitry in the memory interface (Fig 3: #310) is reduced to merely carrying out the command/data from the processor (Fig 3: CPU)).

As in claim 14, Pua discloses the memory controller (Pua's #12) comprises multiples memory interfaces (Fig 1: #15 I/O interface, #16 memory card interface, #17 memory interface,

and memory IC #14) configured to provide additional storage/ memory to the system. Pua does not expressly disclose additional storage/memory as a dynamic random access memory, however, using the dynamic random access memory for storage has been known in the art (see Ganton's paragraph 28 lines 8-11).

Claim 15 rejected based on the same rationale as in claim 13 and 14.

As in claim 16, Ganton discloses the dynamic random access memory is loaded with code (images is stored in SDRAM); this code is readily for used by the CPU. Ganton's paragraph 28 further discloses that the memory controller use the memory in the system in a hierarchical manner. For example, data being paged from/to memory Fig 1: #120 and memory Fig 1: #115).

As in claim 17, Pua discloses removable mass memory (memory attaching to Fig 2: #131 nand ic terminal, #1411 sram ic terminal) provided further information to the fast non-volatile random access memory (Pua's Fig 2: #13) or to sram IC #141 or to both #13 and #141 in response to a further command/information signal provides by the application specific integration circuit (Pua's Fig 2: #12 control IC). Although Pua does not expressly disclose the extend memory sram IC #141 can be a dynamic random access memory. However, a dynamic random access memory can readily be used to extend memory capacity in the system as disclosed by Ganton's paragraph 28 lines 8-11.

As in claim 18, the claim rejected based on the same rationale of claims 14 and 17. Ganton's paragraph 28 further discloses that the memory controller use the memory in the system in a hierarchical manner. For example, data being paged from/to memory Fig 1: #120 and memory Fig 1: #115).

As in claim 34, Pua further discloses the circuitry is integrated into a module (Pua's paragraph 7).

Claim 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (US 6792499), Lin (US 7032105) and Eaton et al (2005/0128322) as applied to claim 1, and in view of Coufal et al (IBM Technical Disclosure Bulletin, Vol 37 No. 11 November 1994, pp 421-424).

As in claim 19, Ganton,Lin, and Eaton do not expressly disclose the fast non-volatile random access memory is a magneto-resistive random access memory, a ferroelectric random access memory, or an Ovonic memory type. However, Coufal discloses a non-volatile random access memory is build as a ferroelectric random access memory (Coufal's first paragraph). It would have been obvious to one of ordinary skill in the art at the time of invention to include a ferroelectric random access memory by Coufal in Ganton's system modified by Lin and Eaton thereby further providing a fast non-volatile random access memory with a huge memory capacity (Coufal's first paragraph, fast access time, and high memory density, third paragraph).

Response to Arguments

Applicant's arguments in response to the last office action has been fully considered but they are not persuasive. Examiner respectfully traverses Applicant's arguments for the following reasons:

A) Regarding Applicant's remarks on page 8 for the rejections of claims 33-34 under 35 U.S.C 112, the amended claims filed 3/2/07 have overcome the rejections.

B) Regarding Applicant's remarks on pages 8-9 for the rejections of claims 1,3-4,8,20-22 and 33 under 35 U.S.C. 102 (e). The arguments are mooted in view of new ground of rejection necessitated by Applicant's amending claims.

C) Regarding Applicant's remarks on page 9 for the rejections of claim 2 under 35 U.S.C. 103 (a), Examiner maintains that Lin discloses the DDR SDRAM as a non-volatile memory by providing a non-interrupt power source, for example a battery, see Lin's Fig 3: #68 SDRAM, column 3 lines 57-62 SDRAM is a non-volatile memory by having an uninterruptible power supply)

D) Regarding Applicant's remarks on pages 9-10 for the rejections of claims 5-7 under 35 U.S.C. 103 (a),

Examiner maintains that any random access memory SRAM, SDRAM etc.. Is non-volatile memory by providing non-interrupt power source as taught by Lin and as discussed in item C.

Examiner maintains that Witek discloses the claims 5,7 limitations as claimed.

Regarding the amended claim 6, Witek does not expressly disclose the frequency ranges corresponding to a core voltage for a memory. However, Micron's page 1, table 2 discloses any memory device with a core frequency capable of operating in a range of frequencies. For example, Table 2: a memory device having an operating frequency ranges 167 MHz to 100 Mhz corresponding to a core voltage for a memory device. It would have been obvious to one of ordinary skill in the art at the time of invention to provide frequency ranges information corresponding to a core voltage of a memory device as suggested by Micron in Ganton's system thereby further allowing the system to optimize the data throughput accordingly to the frequency ranges of the memory device (see Micron's table 2).

E) Regarding Applicant's remarks on pages 10-11 for the rejections of claims 9-11,13-18,34 under 35 U.S.C. 103 (a),

The claims are rejected based on the same rationale as in above paragraphs. Examiner maintains that Pua discloses the additional memory which can be easily connecting to extra connector such as Fig 1: #15 and Fig 1: #17 and to be used directly or indirectly manner. Similarly, Ganton Fig 1, paragraph 29 further discloses the data further can be paged from/to memory area #120 and #115.

F) Regarding Applicant's remarks on page 11 for the rejections of claims 12,19 under 35 U.S.C. 103 (a),

The claims are rejected as discussed in above paragraphs.

G) Regarding Applicant's remarks on pages 11-12 for the motivation. Examiner maintains that the motivation regarding to all rejections are proper. It's noted that Applicant does not point out any specific errors in the motivations regarding the rejections of the claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 36 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.